portion to form a buried oxide layer with respect to the sidewalls". Applicants respectfully submit that the specification clearly defines how the ions pass through the sidewalls of the trench to form a buried oxide layer with respect to the sidewalls. Reference is made in this regard to the paragraph that bridges Pages 18-19 of the instant application. In particular, this paragraph states that plasma immersion ion implantation is an isotropic process for implanting ions show by arrows 164 from an effective non-directional source. This means that the implanting ions are being implanted in all directions into the substrate. Hence, in FIG. 14, ions can be implanted into the sidewalls of the trench in the direction of arrows 164.

The Examiner also states that in Claim 53, lines 1-4 "it is unclear how the trench portions of covered with the first mask to prevent the formation of a buried oxide layer with respect to the sidewalls and bottom of the trench". Also, it is unclear where "the buried oxide is formed with respect to the sidewalls and bottom". Also, 'said covered trench" has no antecedent basis. In response thereto, applicants have amended Claim 53 to positively recite a step of covering a portion of at least one trench having sidewalls that extend to a common bottom wall with said first mask to prevent formation of a buried oxide layer with respect to said sidewalls and common bottom wall of said at least one trench. The amended claim is believed to be definite.

The Examiner also states that in Claim 55, lines 1-3 "it is unclear how the ohmic contacts are formed to the trench sidewalls and bottom of the trench. Also, "said covered trench" has no antecedent basis." In response thereto, applicants have amended Claim 55 to positively recite a step of forming an electrical contact on the sidewalls and bottom of said at least one trench". Support for this amendment to Claim 55 is found in

the last paragraph appearing on Page 17 as well as in FIG. 11. The amended claim is believed to be definite.

In addition to the above amendments, applicants have amended Claim 35 to positively recite that the buried oxide regions and the corresponding SOI layer are formed in a silicon containing substrate. Support for this amendment to Claim 35 is found throughout the specification of the instant application. See, in particular, the drawings that accompany the present application.

Since the above amendments to the claims do not introduce new matter into the specification of the instant application, entry thereof is respectfully requested. Moreover, the above remarks and amendments obviate the §112, second paragraph, rejections; therefore reconsideration and withdrawal thereof are respectfully requested. As required by 37 C.F.R. §1.121, applicants have attached a marked-up copy of the claims showing the changes made by the present amendment.

Claims 35, 40 and 41 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by Japanese Patent No. JP 09064323 A ("JP '323). Claims 36, 38, 39, 42, 43, 44, 45, 46 and 47-50 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of JP '323, U.S. Patent No. 6,063,652 to Kim ("Kim '652") and U.S. Patent No. 5,494,846 to Yamazaki ("Yamazaki").

With respect to the anticipation rejection, it is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the applied prior art reference. Stated another way, the

reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: The absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 U.S.P.Q. 81, 84 (Fed. Cir. 1986).

Applicants submit that Claim 35, 40 and 41 are not anticipated by the disclosure of JP '323 since the applied reference does not disclose a method which includes, among other processing steps, implanting oxygen through openings in a first mask into a silicon containing substrate and thereafter annealing the substrate to form a plurality of first buried oxide regions below a silicon containing layer wherein both the first buried oxide regions and the silicon containing layer are formed into the substrate. In contrast to the present claimed method, JP '323 provides a process that includes the steps of forming a porous Si layer 22 on the surface of a Si containing substrate; forming an epi-Si layer 23 atop the porous Si layer 22; forming a resist 24 having an opening 24A on the epi-Si layer 23; implanting oxygen ions ***into the porous Si layer 22***; and annealing to form buried oxide regions 27 in the substrate.

Applicants observe that in JP '323 the oxygen ions are implanted into a porous Si layer that is deposited atop the substrate. This is different from applicants' claimed processing steps wherein the oxygen ions are implanted into the substrate itself. Thus, JP '323 requires additional processing steps, i.e., separate deposition of a porous Si layer and an epi-Si layer, to form a structure having a buried oxide layer therein.

Applicants submit that JP '323 appears to teach away from forming the buried oxide region in a semiconductor substrate. See the Problem to be Solved portion of the English language Abstract. In JP '323, the problems of forming the buried oxide

directly into the substrate are solved by depositing a porous Si layer and an epi-Si layer atop a substrate; implanting ions into the porous Si layer and then annealing.

The foregoing remarks clearly indicate that the applied reference does not teach each and every aspect of the claimed invention as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of JP '323.

Applicants submit the Claims 36, 38, 39, 42, 43, 44, 45, 46 and 47-50 are not obvious from the combined disclosures of JP '323, Kim '652 and Yamazaki.

Before traversing the §103 rejection citing the combined disclosures of JP '323, Kim '652 and Yamazaki, applicants submit that Kim '652 is effective as prior art as of February 25, 1999 --its effective US filing date--. Applicants assert that Kim '652 is not prior art to the present invention insofar as the present invention was completed in this country before February 25, 1999.

Submitted herewith in this regard is an unsigned copy of a Declaration under 37 C.F.R. §1.131 by all the named inventors of the above-identified patent application.[1] In the 1.131 Declaration, the inventors attest and show by way of attached exhibits that the present invention was completed in the laboratories of IBM Corporation in Yorktown Heights, NY *prior to the February 25, 1999 filing date of Kim '652.*

Clearly, the information provided by the attached 131 Declaration indicates that the present invention was completed by the present applicants in the United States prior to the effective filing date of Kim '652. Consequently, Kim '652 is antedated and cannot be used as a reference against the claims in this application. Therefore, in

[1] A signed copy of the 1.131 Declaration will be submitted in due course.

view of the foregoing, the obviousness rejection is based solely on the disclosures of JP '323 and Yamazaki.

Applicants submit that the combined disclosures of JP '323 and Yamazaki do not render applicants' claimed methods obvious for at least the following reasons.

JP '323 is defective since the principle reference applied does not teach or suggest a method which includes, among other processing steps, implanting oxygen through openings in a first mask into a silicon containing substrate and thereafter annealing the substrate to form a plurality of first buried oxide regions below a silicon containing layer wherein both the first buried oxide regions and the silicon containing layer are formed into the substrate. In contrast to the present claimed method, JP '323 provides a process that includes the steps of forming a porous Si layer 22 on the surface of a Si containing substrate; forming an epi-Si layer 23 atop the porous Si layer 22; forming a resist 24 having an opening 24A on the epi-Si layer 23; implanting oxygen ions ***into the porous Si layer 22***; and annealing to form buried oxide regions 27 in the substrate.

Applicants observe that in JP '323 the oxygen ions are implanted into a porous Si layer that is deposited atop the substrate. This is different from applicants' claimed processing steps wherein the oxygen ions are implanted into the substrate itself. Thus, JP '323 requires additional processing steps, i.e., separate deposition of a porous Si layer and an epi-Si layer, to form a structure having a buried oxide layer therein.

Applicants submit that JP '323 appears to teach away from forming the buried oxide region in a semiconductor substrate. See the Problem to be Solved portion of the English language Abstract. In JP '323, the problems of forming the buried oxide

directly into the substrate are solved by depositing a porous Si layer and an epi-Si layer atop a substrate; implanting ions into the porous Si layer and then annealing. Thus, one skilled in the art would not combine the disclosure of JP '323 with a prior art reference, such as Yamazaki, in which oxygen ions are implanted into the surface of a Si-containing substrate since JP '323 mentions that there are problems associated with such prior art approaches.

Yamazaki, et al. do not render the method recited in Claim 35 obvious since the applied reference does not teach or suggest the formation of a plurality of first buried oxide regions below a silicon contain layer whereby said spaced apart silicon-on-insulator regions are formed. Yamazaki, et al. provide a process in which oxygen ions are partially implanted into a semiconductor substrate to form an oxygen ion implant area. A trench surrounding the oxygen ion implant area is formed to remove outer peripheral portions of the oxygen ion implantation area. Then, the semiconductor substrate is heated to turn the oxygen ion implantation area into a buried oxide film that is stable. In Yamazaki, et al. a single SOI region having a buried oxide layer is formed in the substrate, not a plurality of SOI regions having buried oxide regions as presently claimed such that spaced apart SOI regions are formed on the Si-containing substrate.

The §103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed methods to include applicants' claimed method recited in Claim 35. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of

the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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Registration No. 39,394

LSS/sf
Enclosures Version with markings
Unexecuted Declaration under 1.131

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 35, 53 and 55 have been amended to read as follows:

35. (Amended) A method for forming spaced apart silicon-on-insulator (SOI) regions [on] in an upper region of a silicon containing substrate comprising the steps of:

forming a first mask having openings therein on a surface of said silicon containing substrate,

implanting oxygen through said openings in said first mask into said substrate, and

annealing said substrate to form a plurality of first buried oxide regions below a silicon contain layer, said first buried oxide regions and said silicon containing layer are located in said substrate, whereby said spaced apart silicon-on-insulator regions are formed.

53. (Amended) The method of claim 51 further including the step of covering a portion of at least one trench [portion] having sidewalls that extend to a common bottom wall with said first mask to prevent formation of a buried oxide layer with respect to said sidewalls and common bottom wall of said [covered] at least one trench.

55. (Amended) The method of claim 53 further including the step of forming an [ohmic] electrical contact [with] on the sidewalls and bottom of said [covered] at least one trench.